Applicant has not been given a chance to address any concerns which may have been expressed by the Examiner. The Applicant respectfully requests written notification as to the status of claim 10, and will assume this claim is in condition for allowance unless notified otherwise. If claim 10 (as amended to included the limitations of the base claim 9) stands rejected, the Applicant likewise respectfully requests some written notification to this effect, along with a reasoned statement for the rejection so that a first opportunity to make a proper response is obtained. It should be noted that claim 10 has not been amended for reasons related to patentability, but only to incorporate the text of the cancelled base claim from which claim 10 originally depended.

Rejections Under 35 U.S.C.§102

Claims 1, 4, and 20 were rejected under 35 U.S.C. §102(b) as being clearly anticipated by Hotta et al. (U.S. Patent No. 5,274,829). As claims 1, 4, and 20 have been cancelled, the rejection is now moot. However, the Applicant wishes to note that Hotta et al. does not consistently identify microcode instructions as any particular kind of instruction, and in fact uses the term interchangeably with "macro" instructions and memory access instructions. A prior art reference used in a §102 rejection must be enabling under 35 U.S.C. §112, first paragraph. See Paperless Accounting, Inc. v. Bay Area Rapid Transit Sys., 804 F.2d 659, 665, 231 USPQ 649, 653 (Fed. Cir. 1986), cert denied, 480 U.S. 933 (1987); and In re Moreton, 288 F.2d 708, 711, 129 USPQ 227, 230 (CC.P.A. 1961). The Hotta et al. reference fails in this regard. For example, while Hotta et al. declares that the micro instruction control unit decodes/reads out micro instructions, the unit also reads out macro instructions - both being used to control the computation unit. (Col. 4, lines 50-57). Hotta et al. later asserts that it is the micro instruction control unit which in fact executes micro instructions. (Col. 5, lines 18-21). Similarly, Hotta et al. declares that both the SMIR and MIR registers are used to hold micro instructions, but it appears that only the instruction in the MIR will "cause the computation unit to operate." (Col. 6, line 13 - Col. 7, line 20). This confusing re-interpretation of the term "micro instruction" does not enable one to practice the patented invention, because it is uncertain as to whether microcode, as described in the reference, is really some form of macro-code that is being fetched and

executed. Even giving the Hotta et al. reference the benefit of the doubt, and assuming it is only the latter example which constitutes true "microcode" execution by a processor, it is clear that Hotta et al. fails to describe or teach the operation of processor logic using the Machine Specific Registers *as claimed* by the Applicant. It should also be noted that, while Hotta et al. discloses the possibility of using a cache to store micro instructions, there is no mention of controlling the cache itself using such micro instructions. (Col. 9, line 55 - Col. 10, line 6).

Claims 9 and 13-14 were rejected under 35 U.S.C.§102(b) as being clearly anticipated by Demers et al. (WO 94/12929). As claims 9, and 13-14 have been cancelled, the rejection is now moot. However, the Applicant wishes to note that Demers et al. speaks to executing microcode using a microsequencer 201 (not shown, but located in the datapath decode logic, also not shown) to control the datapath decode logic. (Pg. 5, lines 21-28). The terms "decoding" and "execution" are used interchangeably with respect to microcode. (e.g., Col. 6, lines 18-21). Other than generic assertions of execution, no other mention of microcode execution is made. Thus, Demers et al. also fails to describe or teach the operation of processor logic using the Machine Specific Registers *as claimed* by the Applicant.

Claims 1-2, 15, and 17 were rejected under 35 U.S.C.§102(b) as being clearly anticipated by Dao et al. (U.S. Patent No. 4,928,223). As claims 1-2, 15, and 17 have been cancelled, the rejection is now moot. However, the Applicant wishes to note that Dao et al. does not define microcode in the same way as the Applicant. Dao et al. notes the existence of macro code, microcode, and nanocode. (Col. 1, line 63 - Col. 2, line 8). While the existence of an external microcode ROM is noted, it has its own local bus. Use of a main memory bus, *as claimed* by the Applicant, is specifically avoided. Further, it is noted that the microcode instruction merely defines the starting point of a nanocode instruction sequence. (Col. 35, lines 19-21). The ALU handles nanocode sequencing, and not microcode sequencing. (Col. 37, 42-55). Thus, it is the "nanocode" instructions of Dao et al. which equate to the terms "microcode" functions and "programmed code" used by the Applicant, and the nano code instructions of Dao et al. are not stored in external memory, but in a ROM and PLA integral with the ALU. (Figs. 2 and 15, and Col. 7, lines 3-25).

Claims 1, 5-9, 11-12, 15-16, and 18-19 were rejected under 35 U.S.C.§102(b) as being clearly anticipated by Coon et al. (U.S. Patent No. 5,983,334). As claims 1, 5-9, 11-12, 15-16, and 18-19 have been cancelled, the rejection is now moot. However, the Applicant wishes to note that Coon et al. also does not define microcode in the same way as the Applicant. Dao et al. also notes the existence

of microcode and nanocode, and basic microcode instructions are translated by hardware into nano-instructions. (Col. 16, lines 55-63). In fact, it is the nano-instructions, rather than the microcode which the IEU executes. (Col. 16, lines 63-65). While the existence of an external microcode RAM is noted, such "microcode" is actually a high-level machine language, and clearly differentiated from the "typical" microcode claimed by the Applicant. (Col. 17, lines 6-14). The nano-instructions are not stored in external memory, but in the RISC processor core, or IEU. (Col. 19, lines 63-67).

Rejections Under 35 U.S.C.§103

Claim 3 was rejected under 35 U.S.C.§103(a) as being unpatentable over Hotta et al. (U.S. Patent No. 5,274,829). Claim 17 was rejected under 35 U.S.C.§103(a) as being unpatentable over Dao et al. (U.S. Patent No. 4,928,223). Claims 15-16 were rejected under 35 U.S.C.§103(a) as being unpatentable over Coon et al. (U.S. Patent No. 5,983,334). As claims 3, 15-16, and 17 have been cancelled, the rejection is now moot. However, the Applicant wishes to note the use of a single reference under §103(a), along with Official Notice taken by the Examiner to form these rejections. In each case, no reference is supplied to support the assertions made. Thus, it appears the Examiner is making use of his own personal knowledge, and if such assertions are maintained in future office actions, the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) with respect to such to the declarations made regarding advances in the art of memory and the motivation one of ordinary skill in the art would have to use them in the context of the instant invention.

CONCLUSION

The Applicant respectfully submits that claims 10 and 21-40 are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9592 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

HOWARD CHIN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9592

Date March 27, 2002 By Ann M. McCrackin

Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 27 day of March, 2002.

Jane E. Brockschink
Name

Jane E. Brockschink
Signature